



Docket No. 0756-2296

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Hisashi OHTANI et al.)
Serial No.: 09/837,552)
Filed: April 19, 2001)
For: SEMICONDUCTOR DEVICE AND)
MANUFACTURING METHOD THEREOF)

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Satomi Yumoto, B-310, 304-1, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;
that I am the translator of the attached translation of the above identified application Serial No. 09/837,552 filed on April 19, 2001; and
that to the best of my knowledge and belief the following is a true and correct translation of the above identified application Serial No. 09/837,552 filed on April 19, 2001.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 3 day of August, 2001

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Name: Satomi Yumoto



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[Attention] Commissioner, Patent Office

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METHOD THEREOF

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[Attachment] Specification 1

[Attachment] Drawing 1

[Attachment] Abstract 1

[Proof] required